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Claims

[c1] 1. A method of reducing pattern pitch on a substrate, comprising the steps of:
forming a material layer over the substrate;
forming a hard mask layer over the material layer;
forming a patterned photoresist layer over the hard mask layer to exposed a region;
etching the hard mask layer using the patterned photoresist layer as etching mask, wherein due to the trenching effect, a residual hard mask layer remains in the exposed region and a plurality of micro-trenches are formed at the edges of the residual hard mask layer in the exposed region;
patterning the material layer using the residual hard mask layer as etching mask; and
removing the patterned photoresist layer and the hard mask layer.

[c2] 2. The method of claim 1, wherein the step of forming the hard mask layer over the material layer includes the sub-steps of:
forming a thin mask layer over the material layer; and
forming a thick mask layer over the thin mask layer.

[c3] 3. The method of claim 2, wherein the step of etching the hard mask layer using the patterned photoresist layer includes the sub-steps of:
etching the thick mask layer using the patterned photoresist layer as etching mask, wherein due to the trenching effect, a residual thick hard mask layer remains in the exposed region and the micro-trenches are formed in the thick hard mask layer; and
patterning the thin mask layer using the patterned photoresist layer and the residual thick mask layer as etching mask.

[c4] 4. The method of claim 2, wherein the etching selectivity ratio of the thick mask layer to the thin mask layer is greater than 1.

[c5] 5. The method of claim 2, wherein the etching selectivity ratio of the thin mask layer to the material layer is greater than 10.

[c6] 6. The method of claim 4, wherein the thick mask layer includes a silicon nitride layer.

[c7] 7. The method of claim 4, wherein the thin mask layer includes a silicon oxide layer.

[c8] 8. The method of claim 5, wherein the material layer in-

cludes a polysilicon layer.

[c9] 9. The method of claim 1, wherein after the micro-trenches are formed, an additional isotropic etching step is conducted to regulate the width of the micro-trenches.

[c10] 10. A method of forming a patterned mask for reducing pattern pitch, comprising the steps of:
forming a mask layer over a substrate;
forming a patterned photoresist layer over the mask layer;
etching the mask layer using the patterned photoresist layer as etching mask, wherein due to the trenching effect, a residual mask layer remains in an exposed region and a plurality of micro-trenches are formed at the edges of the residual mask layer in the exposed region; and
removing the patterned photoresist layer.

[c11] 11. The method of claim 10, wherein the mask layer includes a silicon nitride layer.

[c12] 12. The method of claim 10, wherein the mask layer includes a silicon oxide layer.

[c13] 13. The method of claim 10, wherein the step of forming the mask layer over the substrate includes the sub-steps

of:

forming a thin mask layer over the substrate; and

forming a thick mask layer over the thin mask layer.

[c14] 14. The method of claim 13, wherein the step of etching the mask layer using the patterned photoresist layer as etching mask includes the sub-steps of:

etching the thick mask layer using the patterned photoresist layer as etching mask, wherein due to the trenching effect, a residual thick mask layer remains in the exposed region and the micro-trenches are formed in the thick mask layer; and

patterning the thin mask layer using the patterned photoresist layer and the residual thick mask layer as etching mask.

[c15] 15. The method of claim 13, wherein the etching selectivity ratio of the thick mask layer to the thin mask layer is greater than 1.

[c16] 16. The method of claim 15, wherein the thick mask layer includes a silicon nitride layer.

[c17] 17. The method of claim 15, wherein the thin mask layer includes a silicon oxide layer.

[c18] 18. The method of claim 10, wherein after the micro-trenches are formed, an additional isotropic etching step

is conducted to regulate the width of the micro-trenches.

[c19] 19. A method of reducing pattern pitch on a substrate, comprising the steps of:
forming a material layer over the substrate;
forming a patterned mask layer on the material layer;
performing an etching process by using the patterned mask layer as etching mask for forming micro-trenches in the material layer, wherein a residual material layer remains in the exposed region and the micro-trenches are formed along sidewalls of the patterned mask layer; and
removing the patterned mask layer.

[c20] 20. The method of claim 19, wherein the etching process comprises a reactive ion etching process.

[c21] 21. The method of claim 20, wherein the bias power of the reactive ion etching process is lower than 150 W, and the source bias power is higher than 500 W.

[c22] 22. The method of claim 20, wherein the reactive gas of the reactive ion etching process comprises chlorine when the material layer is a polysilicon layer and the patterned mask layer is a silicon oxide layer.